PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 65349-007	**FOR FURTHER ACTION**	See Form PCT/IPEA/416
International application No. PCT/US05/09414	International filing date *(day/month/year)* 21 March 2005 (21.03.2005)	Priority date *(day/month/year)* 22 March 2004 (22.03.2004)
International Patent Classification (IPC) or national classification and IPC IPC: **H03L 1/00**(2007.01) USPC: 331/107A		
Applicant MOBIUS MICROSYSTEMS, INC.		

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 5 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. [X] *(sent to the applicant and to the International Bureau)* a total of 28 sheets, as follows:
      - [ ] sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      - [ ] sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.

   b. [ ] *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) _____ , containing a sequence listing and/or tables related thereto, in electronic form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

[X]	Box No. I	Basis of the report
[ ]	Box No. II	Priority
[ ]	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
[ ]	Box No. IV	Lack of unity of invention
[X]	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
[ ]	Box No. VI	Certain documents cited
[ ]	Box No. VII	Certain defects in the international application
[ ]	Box No. VIII	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
14 October 2005 (14.10.2005)	05 December 2006 (05.12.2006)
Name and mailing address of the IPEA/ US Mail Stop PCT, Attn: IPEA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (571) 273-3201	Authorized officer JOSE G. DEES Telephone No. (571) 272-1607

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/US05/09414

Box No. I Basis of the report

1. With regard to the **language**, this report is based on:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of:

☐ international search (under Rules 12.3 and 23.1(b))

☐ publication of the international application (under Rule 12.4(a))

☐ international preliminary examination (under Rules 55.2(a) and/or 55.3(a))

2. With regard to the **elements** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

☐ the international application as originally filed/furnished

☒ the description:
pages 1-6,8-10,12-15,17-20,22,23,25,30-32 and 34-41 as originally filed/furnished
pages* 7,11,16,21,24,26-29 and 33 received by this Authority on 14 October 2005 (14.10.2005)
pages* NONE received by this Authority on _____

☒ the claims:
pages 42 and 44-46 as originally filed/furnished
pages* NONE as amended (together with any statement) under Article 19
pages* 43 received by this Authority on 14 October 2005 (14.10.2005)
pages* NONE received by this Authority on _____

☒ the drawings:
pages NONE as originally filed/furnished
pages* 1-17 received by this Authority on 14 October 2005 (14.10.2005)
pages* NONE received by this Authority on _____

☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing.

3. ☒ The amendments have resulted in the cancellation of:

☒ the description, pages NONE
☒ the claims, Nos. NONE
☒ the drawings, sheets/figs NONE
☒ the sequence listing (*specify*): NONE
☒ any table(s) related to the sequence listing (*specify*): NONE

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

☐ the description, pages _____
☐ the claims, Nos. _____
☐ the drawings, sheets/figs _____
☐ the sequence listing (*specify*): _____
☐ any table(s) related to the sequence listing (*specify*): _____

** If item 4 applies, some or all of those sheets may be marked "superseded."*

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/US05/09414

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims 21, 24, 27, 32	YES
	Claims 1-20, 22, 23, 25, 28-31	NO
Inventive Step (IS)	Claims 21, 24, 27, 32	YES
	Claims 1-20, 22, 23, 25, 28-31	NO
Industrial Applicability (IA)	Claims 1-32	YES
	Claims NONE	NO

2. Citations and Explanations (Rule 70.7)
Please See Continuation Sheet

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**

Continuation of:

V. 2. Citations and Explanations:

Claims 1-20, 22, 23, 25, and 28-31 lack novelty under PCT Article 33(2) as being anticipated by Duncan (US 2003/0030497).

Duncan disclosed an apparatus for frequency control of a resonator (4505), the resonator adapted to provide a first signal (fout) having a resonant frequency, the apparatus comprising an amplifier (4599) coupleable to the resonator, and a frequency controller (4535) coupled to the amplifier and coupleable to the resonator, the frequency controller adapted to modify (4520) the resonant frequency in response to at least one variables (M4);

wherein the plurality of variables comprise temperature, fabrication process, voltage, and frequency (paragraph 0571);

wherein the amplifier further comprises a negative transconductance amplifier (M1, M2);

wherein the frequency controller is further adapted to modify a current (I) through the negative transconductnace amplifier in response to temperature (4536);

wherein the frequency controller further comprises a current source responsive to temperature (M6);

wherein the current source has one or more configurations selected from a plurality of configurations, the plurality of configurations comprising (at least) CTAT, PTAT, and PTAT2 configurations;

wherein the frequency controller is further adapted to modify a current (4522) through the negative transconductance amplifier to select the resonant frequency (selection is a stable resonant frequency);

wherein the frequency controller is further adapted to modify a transconductance of the negative transconductance amplifier to select the resonant frequency (M3);

wherein the frequency controller is further adapted to modify a current through the negative transconductance amplifier in response to a voltage (4533, a current depends on a capacitance);

wherein the frequency controller is further adapted to modify a transconductance of the negative transconductance amplifier in response to fabrication process variation (4536, M3);

Supplemental Box

wherein the frequency controller is further adapted to modify a current through the negative transconductance amplifier in response to fabrication process variation (I);

wherein the frequency controller further comprises a voltage isolator coupled to the resonator and adapted to substantially isolate the resonator from a voltage variation (substrate, 4522);

wherein the voltage isolator comprises a current mirror (M3-M7);

wherein the current mirror has a cascode configuration (M4-M7);

wherein the resonator is one or more of the following resonators: an inductor and a capacitor configured to form an LC-tank resonator (L, C); and a ceramic resonator, a mechanical resonator, a microelectromechanical resonator, and a film bulk acoustic resonator;

wherein the current source further comprises a first transistor (M4), a second transistor (M5) coupled to the first transistor (M4), a second transistor (M5) coupled to the first transistor, a diode (M6) coupled to the first transistor, and a resistor (R2) coupled the second transistor;

wherein the current (I) provided by the current source is a function of a voltage across the diode and a resistance of the resistor; and

wherein the voltage and the resistance are temperature dependent (paragraph 0547).

Claims 21, 24, 26, 27, and 32 meet the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest the transconductance and current modulation for resonant frequency control and selection as claimed.

Claims 1-32 meet the criteria set out in PCT Article 33(4), and thus have industrial applicability because the subject matter claimed can be made or used in industry.

---------- NEW CITATIONS ----------

NONE

Figure 11 (or "FIG. 11") is a circuit diagram illustrating an exemplary first process variation compensation module in accordance with the teachings of the present invention.

Figure 12 (or "FIG. 12") is a circuit diagram illustrating an exemplary second process variation compensation module in accordance with the teachings of the present invention.

Figure 13 (or "FIG. 13") is a block diagram illustrating an exemplary frequency calibration module in accordance with the teachings of the present invention.

Figure 14 (or "FIG. 14") is a block diagram illustrating an exemplary frequency divider, square wave generator, asynchronous frequency selector and glitch suppression module in accordance with the teachings of the present invention.

Figure 15 (or "FIG. 15") (divided into FIGs. 15A and 15B) is a graphical diagram illustrating exemplary low latency frequency switching in accordance with the teachings of the present invention.

Figure 16 (or "FIG. 16") is a block diagram illustrating an exemplary frequency divider in accordance with the teachings of the present invention.

Figure 17 (or "FIG. 17") is a block diagram illustrating an exemplary power mode selection module in accordance with the teachings of the present invention.

Figure 18 (or "FIG. 18") is a block diagram illustrating an exemplary synchronization module for a second oscillator in accordance with the teachings of the present invention.

Figure 19 (or "FIG. 19") is a flow diagram illustrating an exemplary method in accordance with the teachings of the present invention.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

While the present invention is susceptible of embodiment in many different forms, there are shown in the drawings and will be described herein in detail specific examples and embodiments thereof, with the understanding that the present disclosure is to be considered as an exemplification of the principles of the invention

variations which may be caused due to temperature and/or voltage fluctuations and fabrication process variations.

Fifth, the clock generator and/or timing/frequency reference 100 generates a significantly and comparatively high frequency, such as in the hundreds of MHz and GHz range, which is then divided to a plurality of lower frequencies. Each such division by "N" (a rational number, as a ratio of integers) results in a significant noise reduction, with phase noise reduced by N and noise power reduced by N^2. As a consequence, the clock generator of the present invention results in significantly less jitter than available with other oscillators, such as ring oscillators.

These features are illustrated in greater detail in Figure 2, which is a block diagram illustrating a first exemplary apparatus 200 embodiment in accordance with the teachings of the present invention. As illustrated in Figure 2, the apparatus 200 is a clock generator and/or timing/frequency reference, providing one or more output signals, such as a clock or reference signal having any of a plurality of frequencies, selected using frequency selector 205. The apparatus (or clock generator) 200 includes an oscillator 210 (having a resonant element), a frequency controller 215, a frequency divider 220, a mode selector 225, and the frequency selector 205 mentioned above. In accordance with the invention, the oscillator 210 generates a signal having a comparatively high frequency, f_0. Due to PVT variations mentioned above, the frequency controller 215 is utilized to frequency select or tune the oscillator 210, such that the oscillation frequency f_0 is selectable from a plurality of potential oscillation frequencies, *i.e.*, the frequency controller 215 provides for output signals having frequencies which are accurate over PVT variations.

For example, given these PVT variations, the output frequency from an oscillator, such as oscillator 210, may vary plus or minus 5%. For some applications, such as those utilizing ring oscillators, such frequency variability may be acceptable. In accordance with the present invention, however, greater accuracy for the clock generator 200 is desirable, particularly for more sensitive or complex applications, such as providing clock signals for integrated microprocessors, microcontrollers, digital signal processors, communication controllers, and so on. As a consequence, frequency controller 215 is utilized to adjust for these PVT variations, such that the output frequency from the oscillator is the selected or desired frequency f_0 with much less

fabricated integrally and monolithically with other circuitry, such as the second circuitry 180, and provides a distinct advantage of the present invention.

In addition, the capacitance 440 illustrated in Figure 4 is only a portion of the overall capacitance involved in the resonance and frequency determination of the resonant LC tank 405, and is a fixed capacitance. In selected embodiments, this fixed capacitance may represent approximately 10% to 90% of the total capacitance ultimately utilized in the oscillator, as an example. As discussed in greater detail below, the overall capacitance is distributed, such that additional fixed and variable capacitance is selectively included within the clock generator and/or timing/frequency reference 300, and is provided, for example, by temperature-responsive frequency (f_0 (T)) compensation module 420 and process variation compensation module 425, to provide for both selecting the resonant frequency f_0 and to allow the resonant frequency f_0 to be substantially independent of both temperature and process variations.

In the selected embodiments, the inductance 435 has been fixed, but also could be implemented in a variable manner, or as a combination of fixed and variable inductances. As a consequence, those of skill in the art will recognize that the detailed discussions of fixed and variable capacitance, for both frequency tuning and temperature and process independence, pertain similarly to inductance choices. For example, different inductances could be switched in or out of the oscillator, to similarly provide tuning. In addition, a single inductor's inductance may also be modulated. As a consequence, all such inductance and capacitance variations are within the scope of the present invention.

Also as illustrated in Figure 4, the resonant LC tank 405 and resulting output signal, referred to as a first (output) signal at nodes or lines 470 and 475, is a differential signal and provides common-mode rejection. Other configurations, including non-differential or other single-ended configurations are also within the scope of the present invention. For example, in single-ended configurations, only one instantiation of the various modules (*e.g.*, 485, 460) would be required, rather than the use of two for a balanced configuration as illustrated. Similarly, other components and features discussed below, such as frequency dividers, would also have a single-ended rather than differential configuration. In addition, various embodiments illustrated utilize MOSFET transistors in various forms (such as CMOS, AMOS,

M4) sizing should be jointly selected to provide for oscillation start up, to accommodate maximum currents for power consumption constraints, and to fit into the selected IC area and layout. For example, the transconductance g_m may be selected to provide approximately sufficient current to ensure start up and sustain oscillation, with a frequency characteristic of decreasing frequency with increasing temperature, followed by sizing transistors M1, M2, M3 and M4 to be large enough to either make the frequency independent of temperature or increasing with increasing temperature, followed by fine-tuning the frequency-temperature relationship with appropriate selection of I(T). In selected modeled embodiments, this has resulted in frequency accuracy of approximately ± 0.25% to 0.5 % over PVT, which may be more than sufficient for many applications.

Referring again to Figure 4, additional compensation modules are also utilized to provide greater control and accuracy over the resonant frequency f_0, such as for applications in which greater accuracy and less variance (or frequency drift) may be required, or where technologies do not allow the previous techniques to provide sufficient accuracy over PVT variations, such as to provide a frequency accuracy of approximately ± 0.25 % or better. In these circumstances, temperature-dependent (or temperature-responsive) frequency (f_0(T)) compensation module 420 may be utilized, such as the exemplary temperature-responsive frequency (f_0(T)) compensation module 420. This module 420 may be implemented, for example, utilizing controllable capacitance modules 485, with each coupled to a respective side or rail of the resonant LC tank 405 (lines 470 and 475), and with each under common control, provided by a first plurality ("w") of switching coefficients (p_0 though $p_{(w-1)}$) (register 495) and a voltage controller (V_{CTRL}) 480 providing a control voltage determined by a second plurality ("x") of switching coefficients (q_0 though $q_{(x-1)}$) (register 455), with representative examples illustrated in Figures 9 and 10.

Figure 9 is a circuit diagram illustrating an exemplary controllable capacitance module 635 in accordance with the teachings of the present invention, which may be utilized as the controllable capacitance modules 485 in the frequency-temperature compensation module 420 (and attached to each side of the resonant LC tank 405 (nodes or lines 470 and 475)). As illustrated, the controllable capacitance module 635 is comprised of a bank or array of a plurality (w) of switchable capacitive

combinations of coefficients, to provide a finer level of adjustment, resulting in a substantially and significantly flat frequency response as a function of varying ambient temperature. The first and second pluralities of coefficients are then loaded into respective registers 495 and 455 in all of the ICs fabricated in the selected processing run (or batch). Depending on the fabrication processing, under other circumstances, it is possible that for higher accuracy, each IC may be separately calibrated. As result, in conjunction with the temperature compensation provided by the negative transconductance amplifier 410 and I(T) generator 415, the overall frequency response of the clock generator is substantially independent of temperature fluctuations.

As a consequence, the overall capacitance provided to the resonant LC tank 405 is distributed into a combination of fixed and variable portions, with the variable portions responsive to provide temperature compensation and, therefore, control over the resonant frequency f_0. The more variable capacitance C_v which is switched into the circuit (controlled capacitor module 635), the greater the response to fluctuations in ambient temperature.

In addition to providing temperature compensation, it should be noted that a switched or controllable capacitance module 635 may also be utilized to select or tune the resonant frequency f_0.

Referring again to Figure 4, another compensation module is also utilized to provide greater control and accuracy over the resonant frequency f_0, also for applications in which greater accuracy and less variance (or frequency drift) may be required, such as to provide a frequency accuracy of approximately ± 0.25 % or better over PVT. In these circumstances, a process variation compensation module 425 may be utilized, to provide control over the resonant frequency f_0 independently of fabrication process variations, such as the exemplary modules illustrated in Figures 11 and 12.

Figure 11 is a circuit diagram illustrating an exemplary first process variation compensation module 760 in accordance with the teachings of the present invention. The first process variation compensation module 760 may be utilized as the process compensation modules 460 in Figure 4, with each module attached to a rail or side of the resonant LC tank 405 (lines 470 and 475). In addition, each first process variation compensation module 760 is controlled by a third plurality ("y") of switching

to include the corresponding fixed capacitance 750, and could be "blown" (open-circuited) to remove the corresponding fixed capacitance 750 from the resonant LC tank 405.

Figure 12 is a circuit diagram illustrating an exemplary second process variation compensation module 860 in accordance with the teachings of the present invention. The second process variation compensation module 860 may be utilized as the process compensation modules 460 in Figure 4, with each module attached to a rail or side (lines 470 and 475) of the resonant LC tank 405, instead of modules 760. In addition, each second process variation compensation module 760 would also be controlled by a third plurality of switching coefficients r_0 though $r_{(y-1)}$, stored in register 465. (Because of the different circuitry employed in each exemplary process variation compensation module 760 or 860, however, the corresponding third pluralities of switching coefficients r_0 though $r_{(y-1)}$ would, of course, be different from each other.)

It should be noted that Figure 12 provides a varactor illustration different from those utilized in other Figures, in which a varactor 850 is represented by a MOS transistor, rather than as a capacitor with an arrow through it. Those of skill in the art will recognize that varactors are often A-MOS or I-MOS transistors, or more generally MOS transistors, such as those illustrated in Figure 12, and configured by shorting the transistor's source and drain. As a consequence, the other illustrated varactors may be consider to include, as potential embodiments, the A-MOS or I-MOS transistors as configured as in Figure 12. In addition, the varactors 850 are also binary-weighted with respect to each other.

The second process variation compensation module 860 has a similar structural concept, but additional notable differences from the first process variation compensation module 760. The second process variation compensation module 860 provides an array or bank of a plurality of switchable variable capacitive modules 865, without MOS switches/transistors, and hence the losses or loading through the MOS transistors are eliminated. Instead, the load appears as a low loss capacitance; such low loss also implies that the oscillator start-up power is less. In the second process variation compensation module 860, a MOS varactor 850 is switched either to ground or the power rail (voltage V_{DD}), thereby providing either the minimum capacitance or the maximum capacitance to the resonant LC tank 405 based upon the varactor 850

geometry. For AMOS, switched to voltage V_{DD} would provide minimum capacitance and switched to ground would provide maximum capacitance, while the opposite is the case for IMOS. Again, the second process variation compensation module 860 is comprised of an array of binary-weighted variable capacitances, as varactors 850, for adjustment and selection of the resonant frequency f_0, by coupling a selected varactor 850 to ground or V_{DD}, through a corresponding "r" coefficient.

As each capacitance branch is switched to ground or V_{DD}, the corresponding variable capacitance is added to or not included in the total capacitance available for oscillation in the resonant LC tank, thereby modulating the resonant frequency. More particularly, for an A-MOS implementation, coupling to V_{DD} (as V_{in}) provides lesser capacitance and coupling to ground ($V_{in} = 0$) provides greater capacitance, with the opposite holding for an I-MOS implementation, in which coupling to V_{DD} (as V_{in}) provides greater capacitance and coupling to ground ($V_{in} = 0$) provides lesser capacitance, where it is assumed that the voltage on the rails of the LC tank (nodes or lines 470 and 475 of Figure 4) is between zero V and voltage V_{DD}, and significantly or substantially far from either voltage level. The third plurality of switching coefficients r_0 though $r_{(y-1)}$ is also determined post-fabrication using test ICs, also generally as an iterative process with the determinations of the first and second pluralities of switching coefficients. The determined "r" coefficients are then stored in the corresponding registers 465 of the ICs of that production or process batch. Again, individual ICs may also be calibrated and tested separately.

It should also be noted that the illustrated embodiments for modules such as temperature compensator 315 (or 410 and 415) and process variation compensator 320 (or 425 and 460), such as those illustrated in Figures 6 – 12, may be utilized for other purposes. For example, the various illustrated embodiments for the compensator 315 (or 410 and 415) may be made dependent upon process variation, rather than temperature. Similarly, the various illustrated embodiments for the compensator 320 (or 425 and 460) may be made dependent upon temperature, rather than process variation. As a consequence, the embodiments for these and other modules should not be considered limited to the exemplary circuits and structures illustrated, as those of skill in the art will recognize additional and equivalent circuits and applications, all of which are within the scope of the invention.

Referring again to Figures 3 and 4, the clock generator and/or timing/frequency reference 300 may also include a frequency calibration module (325 or 430). This frequency calibration module is the subject of a separate patent application, but its high-level functionality is described briefly below. Figure 13 is a high-level block diagram illustrating an exemplary frequency calibration module 900 (which may be utilized as module 325 or 430) in accordance with the teachings of the present invention. The frequency calibration module 900 includes a digital frequency divider 910, a counter-based frequency detector 915, a digital pulse counter 905, and a calibration register 930 (which also may be utilized as register 465). Using a test IC, the output signal from the clock generator (200 or 300) is frequency divided (910) and compared with a known reference frequency 920 in frequency detector 915. Depending upon whether the clock generator (200 or 300) is fast or slow with respect to the reference, down or up pulses are provided to the pulse counter 905. Based upon those results, the third plurality of switching coefficients r_0 though $r_{(y-1)}$ is determined, and the clock generator (200 or 300) is calibrated to a selected reference frequency. Again, individual ICs may also be calibrated and tested separately.

Referring again to Figures 2, 3 and 4, it will be appreciated by those of skill in the art that a highly accurate over PVT, low jitter, free-running and self-referenced oscillator has been described, providing a differential, substantially sinusoidal signal having a selectable and tunable resonant frequency, f_0, available at nodes 470 and 475. For many applications, this signal is sufficient, and may be utilized directly (and may be output on line 250 of Figure 2, or line 350 of Figure 3, or between the rails or lines 470 and 475 of Figure 4). For example, this signal may be utilized as a timing or frequency reference. In accordance with the present invention, additional applications are available, including clock generation (substantially square wave), frequency division, low-latency frequency switching, and mode selection, as described below.

Figure 14 is a block diagram illustrating an exemplary frequency divider and square wave generator 1000, and an exemplary asynchronous frequency selector 1050, with exemplary glitch suppression module 1080 in accordance with the teachings of the present invention. As indicated above, frequency divider and square wave generator 1000 may be included in or comprise modules 220 and/or 330, and frequency

selector 1050 (with or without glitch suppression module 1080) may be included in or comprise modules 205 and/or 335.

Referring to Figure 14, the output signal from the oscillator, namely, a substantially sinusoidal signal having a frequency f_0, such as output on line 250 of Figure 2, or line 350 of Figure 3, or between the rails or lines 470 and 475 of Figure 4, is input into frequency divider and square wave generator 1000. The frequency of this substantially sinusoidal signal is divided by any one or more arbitrary values "N" into "m" different frequencies (including f_0, where appropriate), and converted to substantially square wave signals, resulting in a plurality of substantially square wave signals having m + 1 different available frequencies, output on lines or bus 1020 as frequencies f_0, f_1, f_2, through f_m. Any of these substantially square wave signals having m + 1 different available frequencies are selectable asynchronously through exemplary asynchronous frequency selector 1050 which, as illustrated, may be embodied as a multiplexer. The selection of any of these substantially square wave signals having m + 1 different available frequencies may be accomplished through the plurality of selection lines (S_m through S_0) 1055, providing a substantially square wave signal having the selected frequency, output on line 1060.

As part of asynchronous frequency selection, glitch suppression is also provided by glitch suppression module 1080, which may be embodied in a plurality of ways, including through the use of one or more exemplary D flip-flops ("DFFs") illustrated in Figure 14. A glitch could occur in an asynchronous frequency transition in which either a low state or a high state is not maintained for a sufficient period of time and may cause metastability in circuitry which is driven by the output clock signal. For example, an asynchronous frequency transition could result in a low state at a first frequency transitioning into a high state at a second frequency, at a point where the high state is about to transition back to a low state at the second frequency, resulting in a voltage spike or glitch. To avoid potential glitches from being provided as part of an output clock signal, the selected substantially square wave signal (having the selected frequency) is provided on line 1060 to a first DFF 1065 which provides a holding state; if a glitch should occur, it will be held until a clock edge triggering the DFF. To avoid the glitch occurring at the clock edge, the DFFs may be clocked at less than the maximum available frequency, or one or more additional DFFs (such as DFF

synchronization, a pulsed-synchronization may also be provided, in which the clock generator and/or timing/frequency reference (100, 200 or 300) provides a pulsed output, and synchronization occurs during the interval of these pulses, as a synchronization interval.

Figure 19 is a flow diagram illustrating an exemplary method in accordance with the teachings of the present invention, and provides a useful summary. The method begins with start step 1220, such as through clock generator and/or timing/frequency reference (100, 200 or 300) start-up. It should be noted that while illustrated in Figure 19 as consecutive steps, these steps may occur in any order, and generally may occur concurrently as the clock generator and/or timing/frequency reference (100, 200 or 300) operates. Referring to Figure 19, a resonant signal having a resonant frequency is generated, step 1225, such as through LC tank 405 or resonator 310. The resonant frequency is adjusted in response to temperature, step 1230, such as through a temperature compensator 315, which adjusts current and frequency. The resonant frequency is adjusted in response to fabrication process variation, step 1235, such as through process variation compensator 320. The resonant signal having the resonant frequency is divided into a plurality of second signals having a corresponding plurality of frequencies, in which the plurality of frequencies are substantially equal to or lower than the resonant frequency, step 1240, such as through frequency divider 330 or 1000). An output signal is selected from the plurality of second signals, step 1245, such as through frequency selector 335 or 1050, for example. Depending upon the selected embodiment or mode, the selected output signal may be provided directly, for example, as a reference signal.

In other embodiments, such as when the output signal is a differential rather than single-ended signal, and when the resonant signal is a substantially sinusoidal signal, the method continues with converting the differential, substantially sinusoidal signal to a single-ended, substantially square wave signal having a substantially equal high and low duty cycle, as needed, step 1250, such as to generate a clock output signal using modules 330 or 1000, for example. An operating mode is also selected from a plurality of operating modes, step 1255, where the plurality of operating modes can be selected from a group comprising a clock mode, a timing and frequency reference mode, a power conservation mode, and a pulse mode, for example,

8. The apparatus of claim 3, wherein the frequency controller is further adapted to modify a transconductance of the negative transconductance amplifier to select the resonant frequency.

9. The apparatus of claim 3, wherein the frequency controller is further adapted to modify a current through the negative transconductance amplifier in response to a voltage.

10. The apparatus of claim 3, wherein the frequency controller is further adapted to modify a transconductance of the negative transconductance amplifier in response to fabrication process variation.

11. The apparatus of claim 3, wherein the frequency controller is further adapted to modify a current through the negative transconductance amplifier in response to fabrication process variation.

12. The apparatus of claim 1, wherein the frequency controller further comprises a voltage isolator coupled to the resonator and adapted to substantially isolate the resonator from a voltage variation.

13. The apparatus of claim 12, wherein the voltage isolator comprises a current mirror.

14. The apparatus of claim 13, wherein the current mirror has a cascode configuration.

15. The apparatus of claim 1, wherein the resonator is one or more of the following resonators: an inductor (L) and a capacitor (C) configured to form an LC-tank resonator; a ceramic resonator, a mechanical resonator, a microelectromechanical resonator, and a film bulk acoustic resonator.

FIG. 1

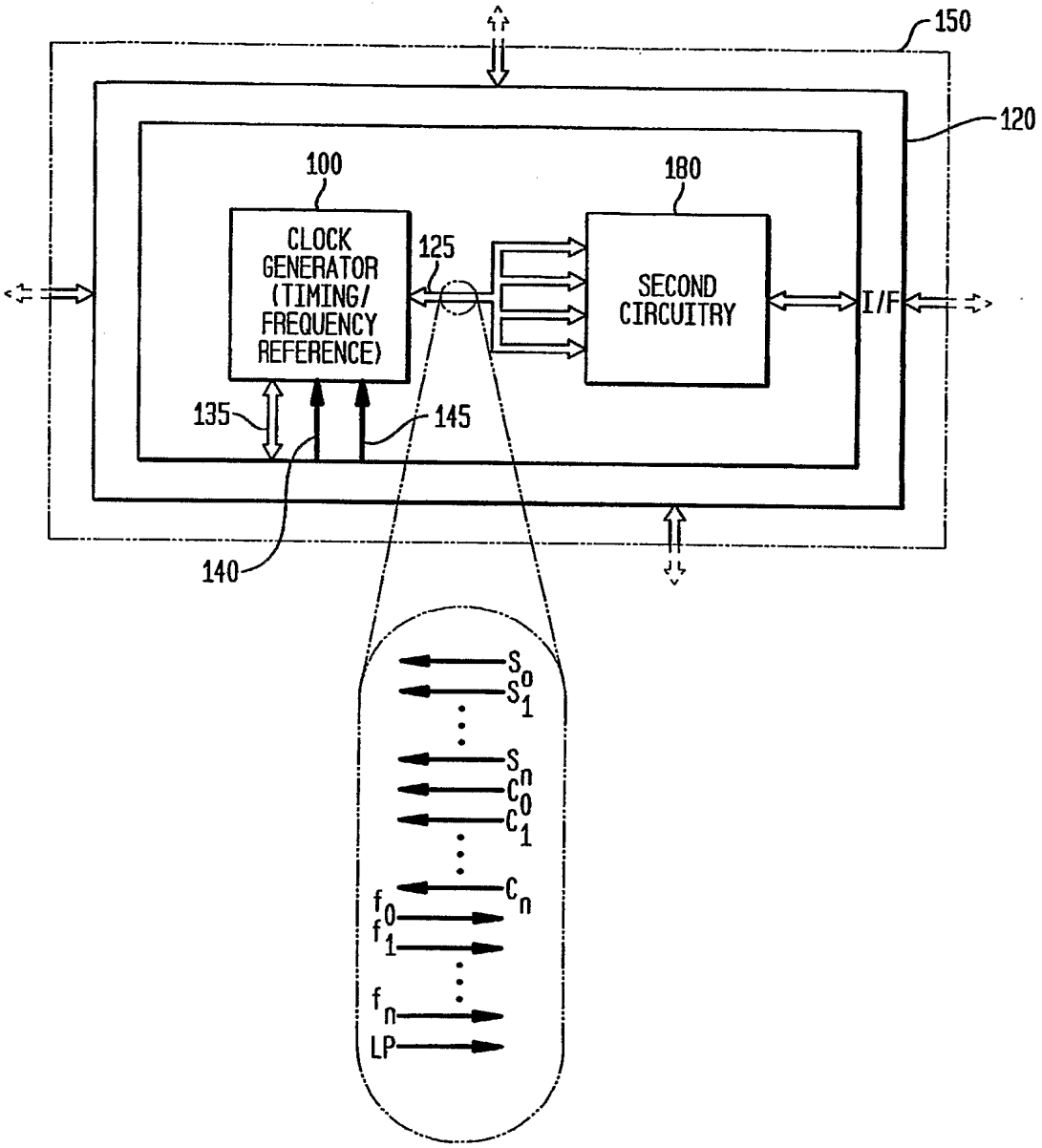

150
120
100
180
CLOCK GENERATOR (TIMING/ FREQUENCY REFERENCE)
125
SECOND CIRCUITRY
I/F
135
145
140
S_0
S_1
S_n
C_0
C_1
C_n
f_0
f_1
f_n
LP

FIG. 2

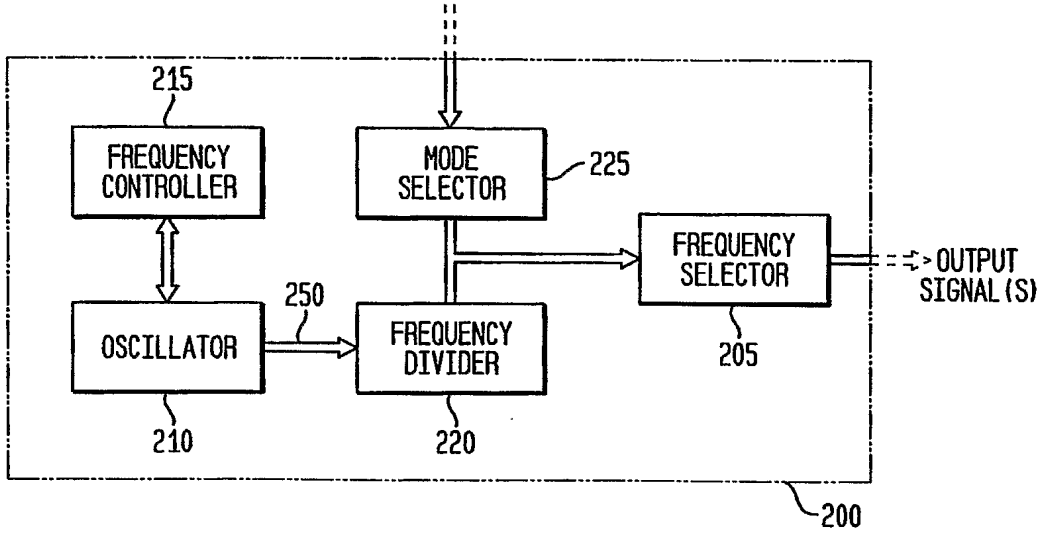
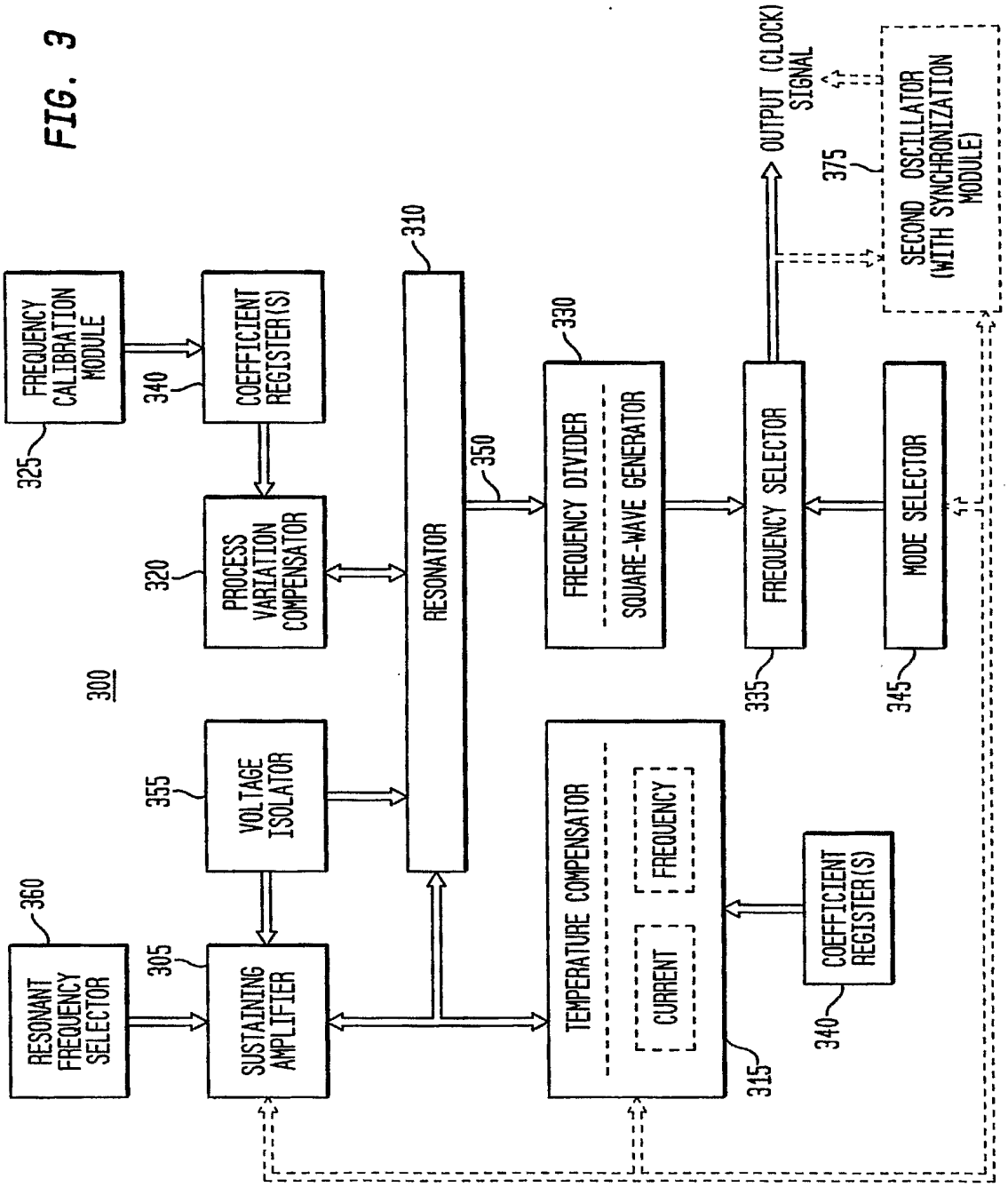

215
FREQUENCY CONTROLLER
MODE SELECTOR
225
FREQUENCY SELECTOR
OUTPUT SIGNAL(S)
250
OSCILLATOR
FREQUENCY DIVIDER
205
210
220
200

FIG. 3


300
FREQUENCY CALIBRATION MODULE
325
COEFFICIENT REGISTER(S)
340
PROCESS VARIATION COMPENSATOR
320
VOLTAGE ISOLATOR
355
RESONANT FREQUENCY SELECTOR
360
SUSTAINING AMPLIFIER
305
RESONATOR
310
350
FREQUENCY DIVIDER
SQUARE-WAVE GENERATOR
330
TEMPERATURE COMPENSATOR
CURRENT
FREQUENCY
315
COEFFICIENT REGISTER(S)
340
FREQUENCY SELECTOR
335
MODE SELECTOR
345
OUTPUT (CLOCK) SIGNAL
375
SECOND OSCILLATOR (WITH SYNCHRONIZATION MODULE)

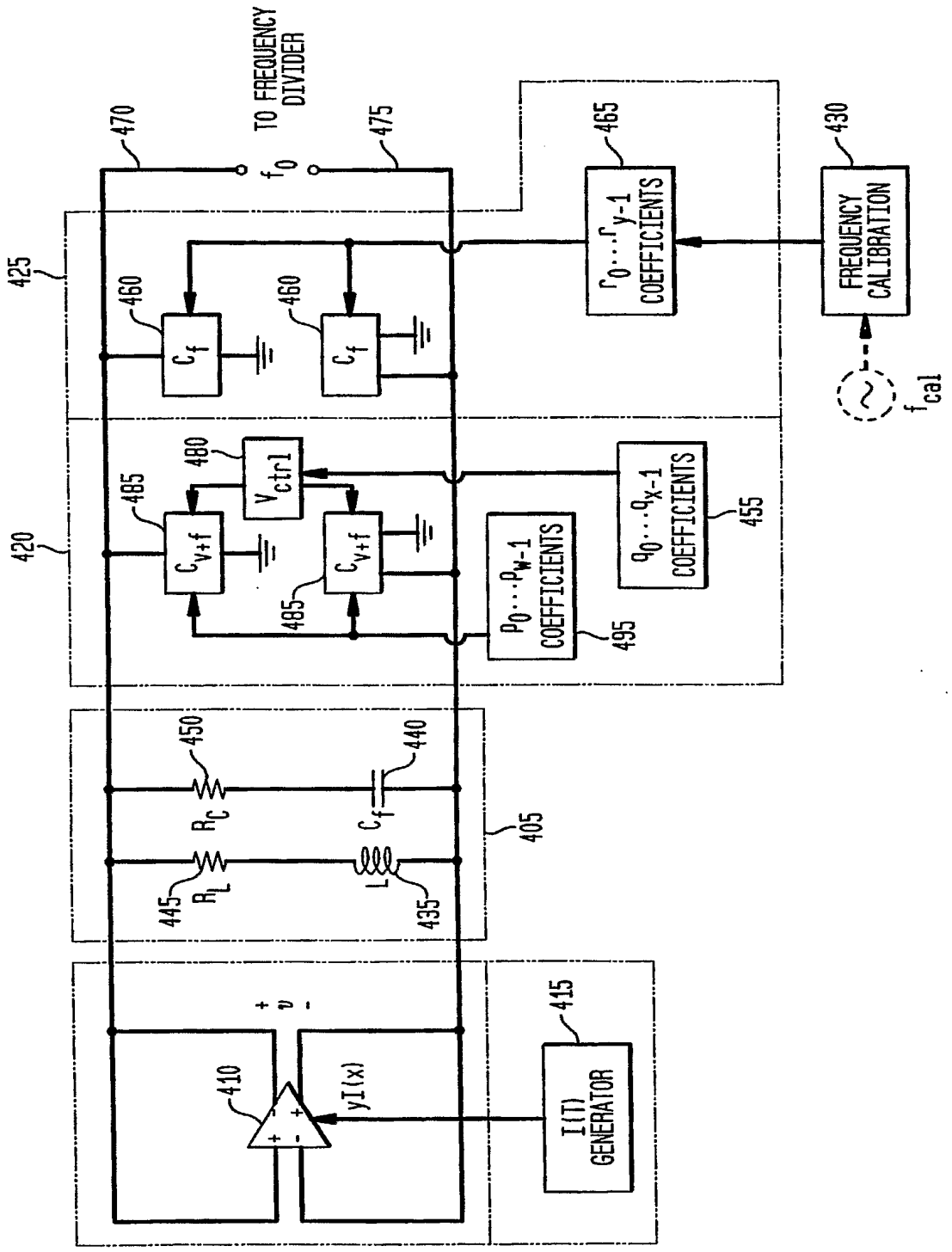

TO FREQUENCY DIVIDER
f_0
470
475
465
430
425
460
460
C_f
C_f
$r_0 \cdots r_{y-1}$ COEFFICIENTS
FREQUENCY CALIBRATION
f_{cal}
480
V_{ctrl}
485
485
C_{v+f}
C_{v+f}
420
$p_0 \cdots p_{w-1}$ COEFFICIENTS
495
$q_0 \cdots q_{x-1}$ COEFFICIENTS
455
450
440
R_C
C_f
405
445
R_L
L
435
+
v
-
410
yI(x)
415
I(T) GENERATOR

FIG. 4

FIG. 5A

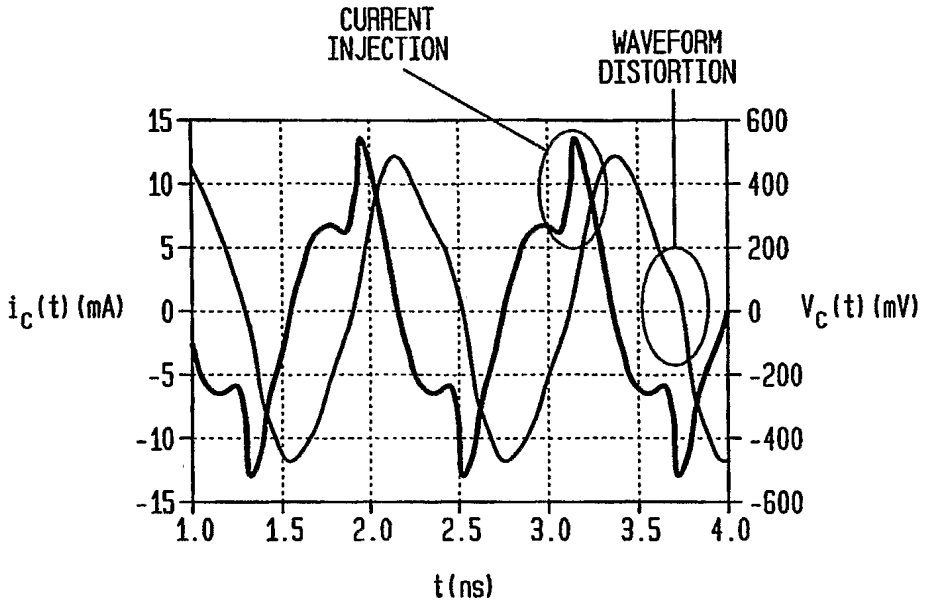
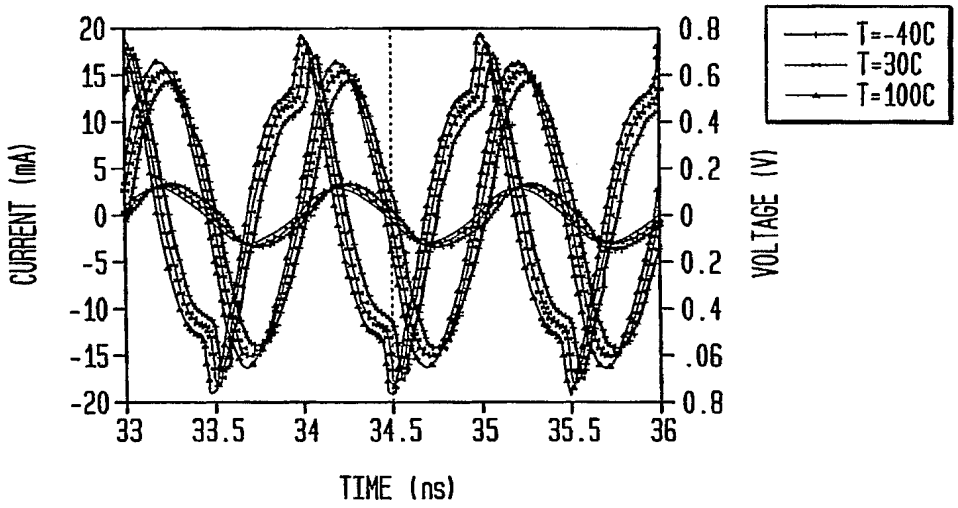


FIG. 5B



TEMPERATURE/BIAS DEPENDENCE

FIG. 5C

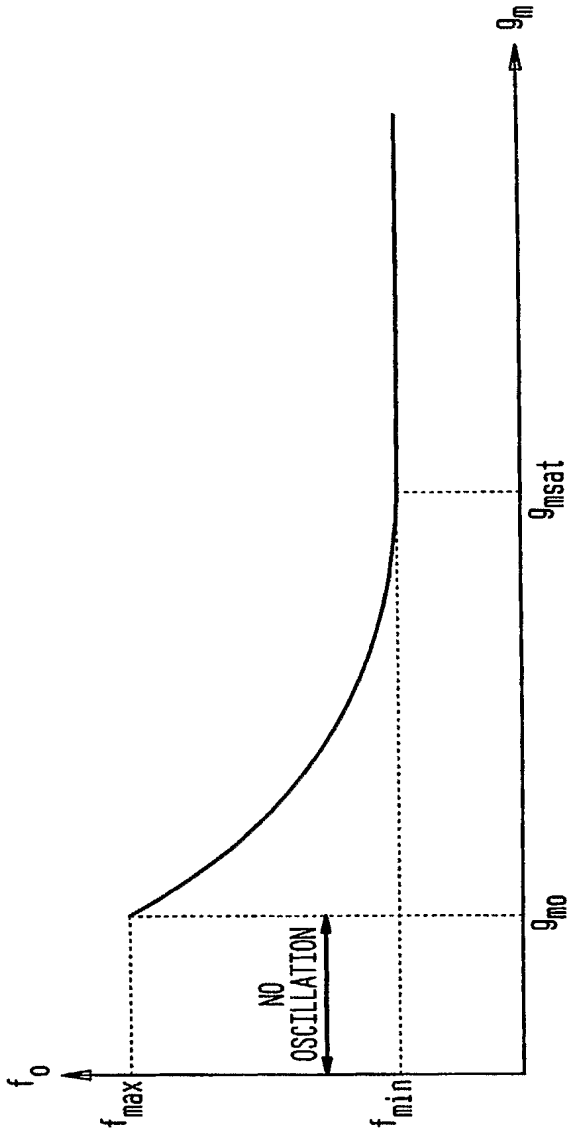


FIG. 6

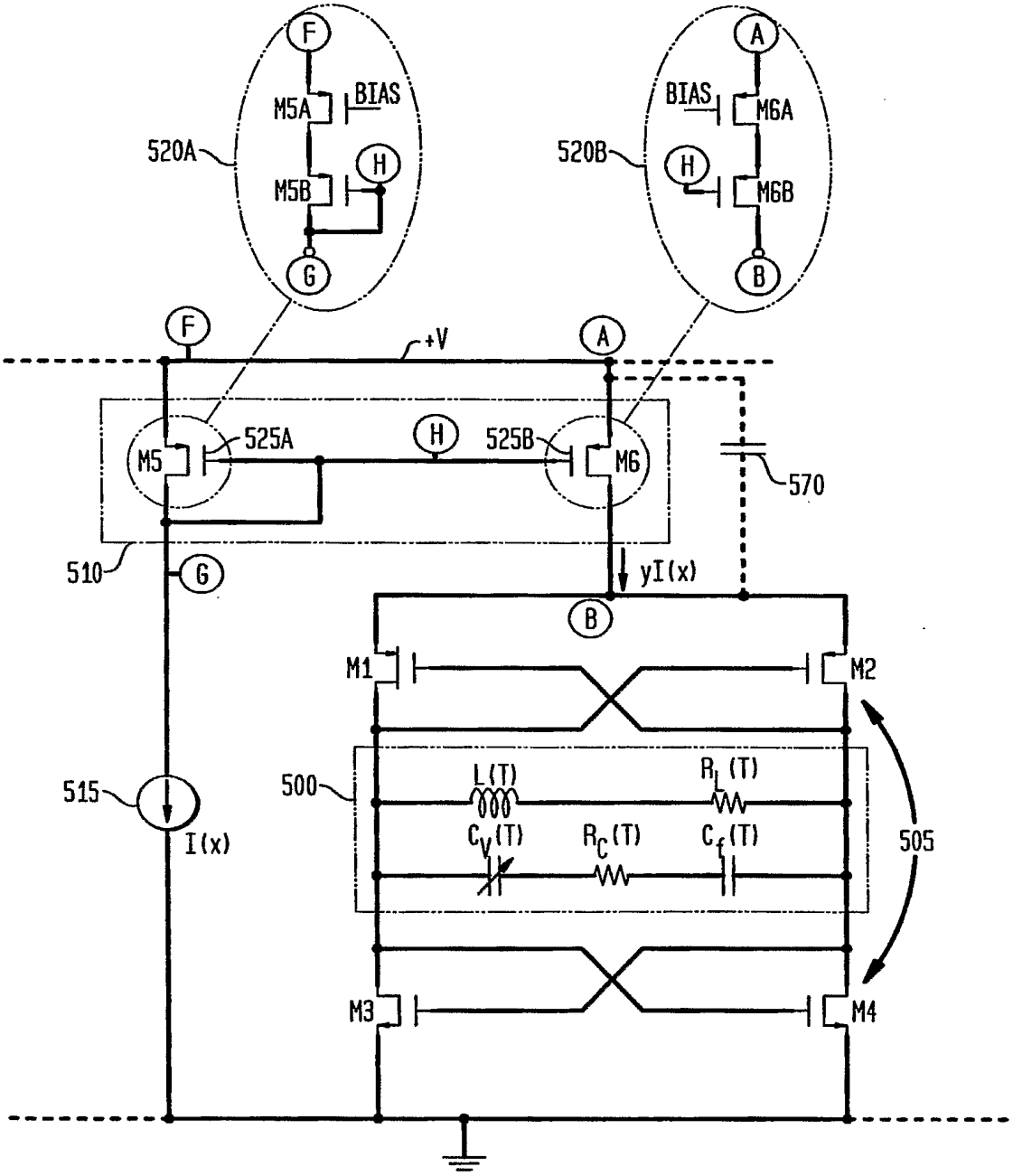

F
M5A
BIAS
520A
H
M5B
G
A
BIAS
M6A
520B
H
M6B
B
F
+V
A
M5
525A
H
525B
M6
570
510
G
yI(x)
B
M1
M2
515
I(x)
500
L(T)
R_L(T)
C_V(T)
R_C(T)
C_f(T)
505
M3
M4

FIG. 7A

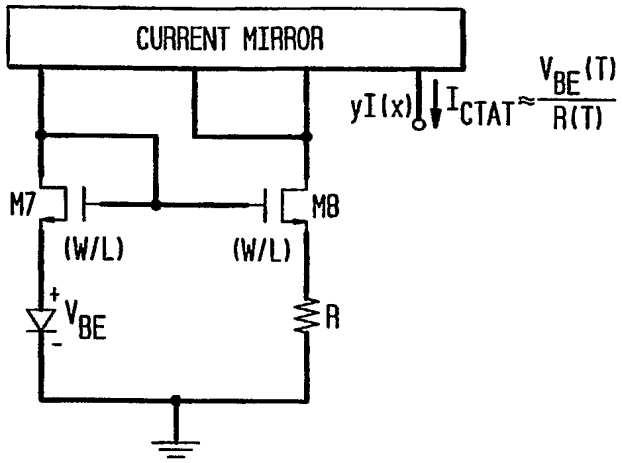

CURRENT MIRROR
yI(x)
$I_{CTAT} \approx \frac{V_{BE}(T)}{R(T)}$
M7
M8
(W/L)
(W/L)
+
V_{BE}
-
R

FIG. 7B

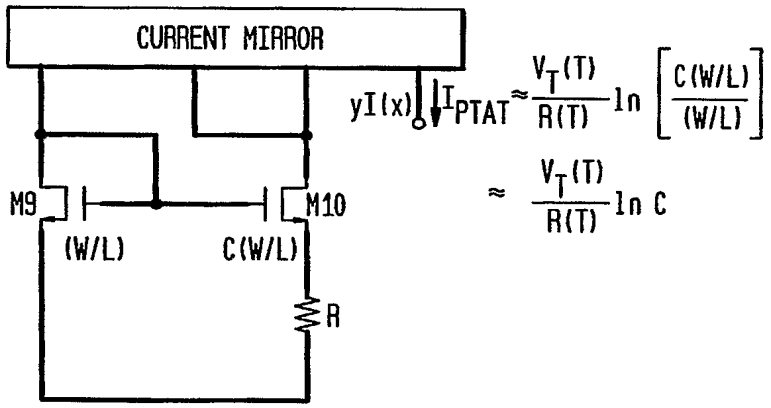

CURRENT MIRROR
yI(x)
$I_{PTAT} \approx \frac{V_T(T)}{R(T)} \ln \left[\frac{C(W/L)}{(W/L)}\right]$
$\approx \frac{V_T(T)}{R(T)} \ln C$
M9
M10
(W/L)
C(W/L)
R

FIG. 7C

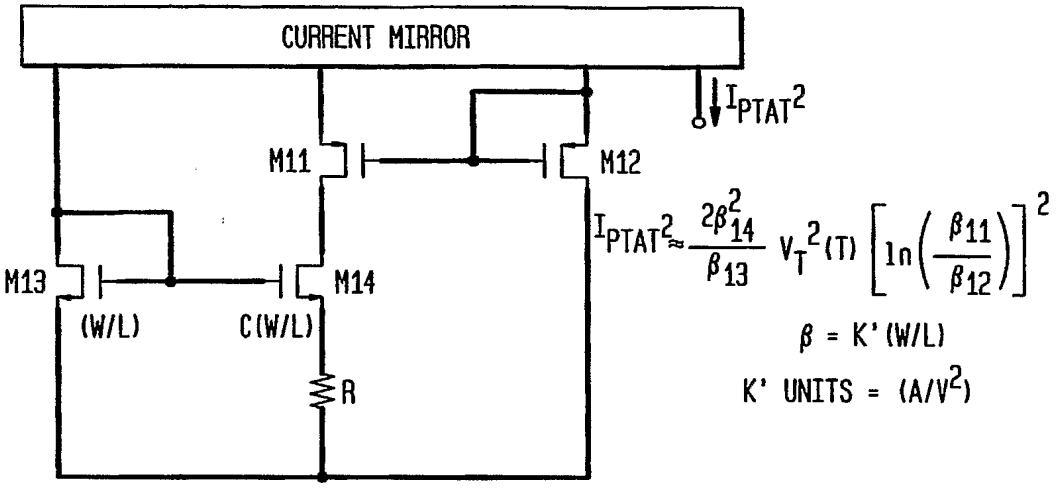

CURRENT MIRROR
I_{PTAT}^2
M11
M12
M13
M14
(W/L)
C(W/L)
R
$I_{PTAT}^2 \approx \frac{2\beta_{14}^2}{\beta_{13}} V_T^2(T) \left[\ln\left(\frac{\beta_{11}}{\beta_{12}}\right)\right]^2$
$\beta = K'(W/L)$
K' UNITS = (A/V^2)

FIG. 7D

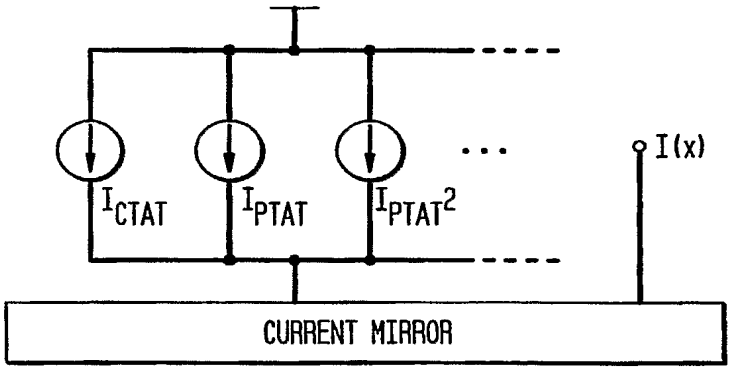

I_{CTAT}
I_{PTAT}
I_{PTAT}^2
I(x)
CURRENT MIRROR

FIG. 8

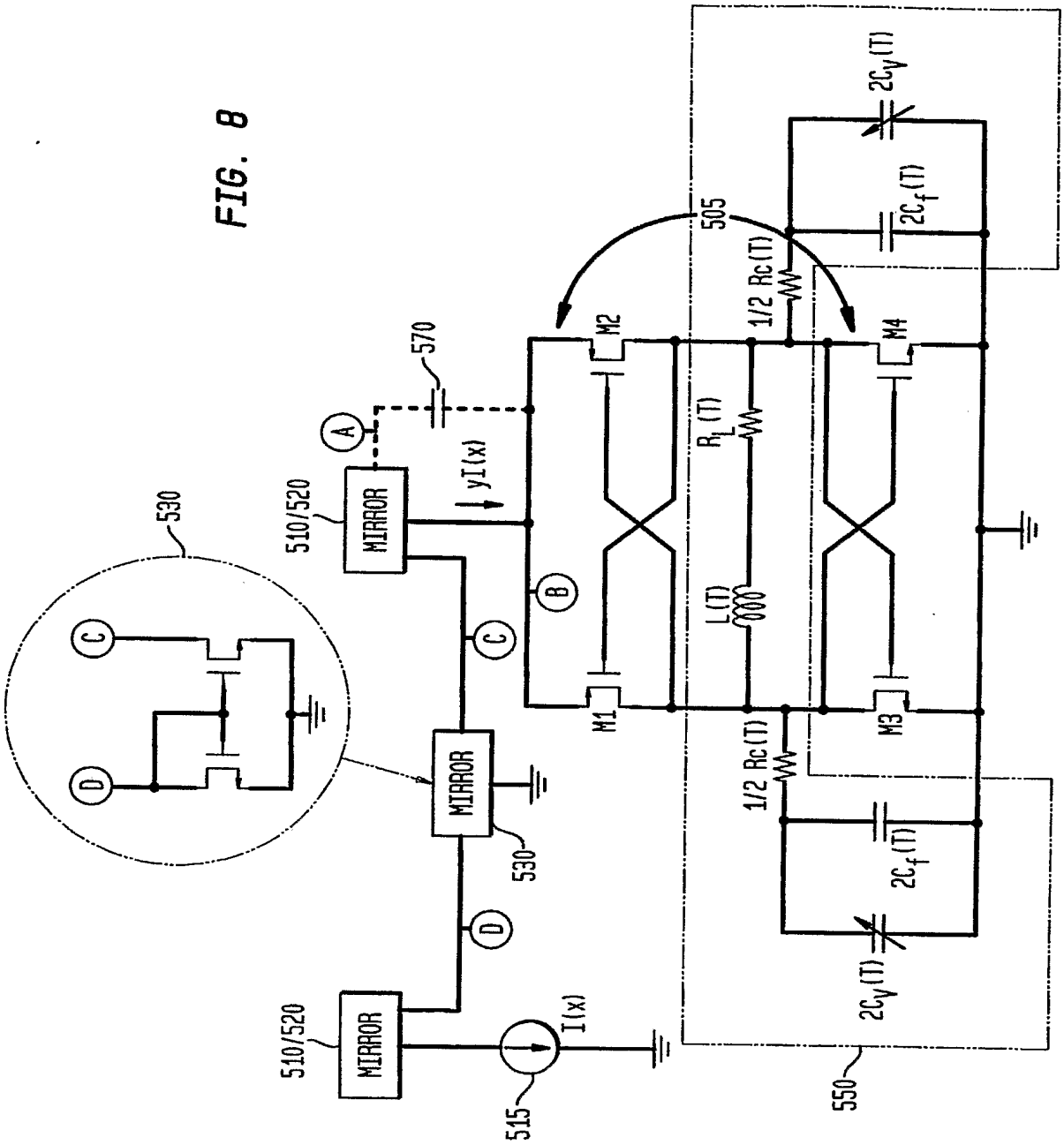

505
570
530
510/520
MIRROR
yI(x)
I(x)
515
550
M1
M2
M3
M4
1/2 Rc(T)
R_L(T)
L(T)
$2C_f$(T)
$2C_y$(T)
A
B
C
D

FIG. 9

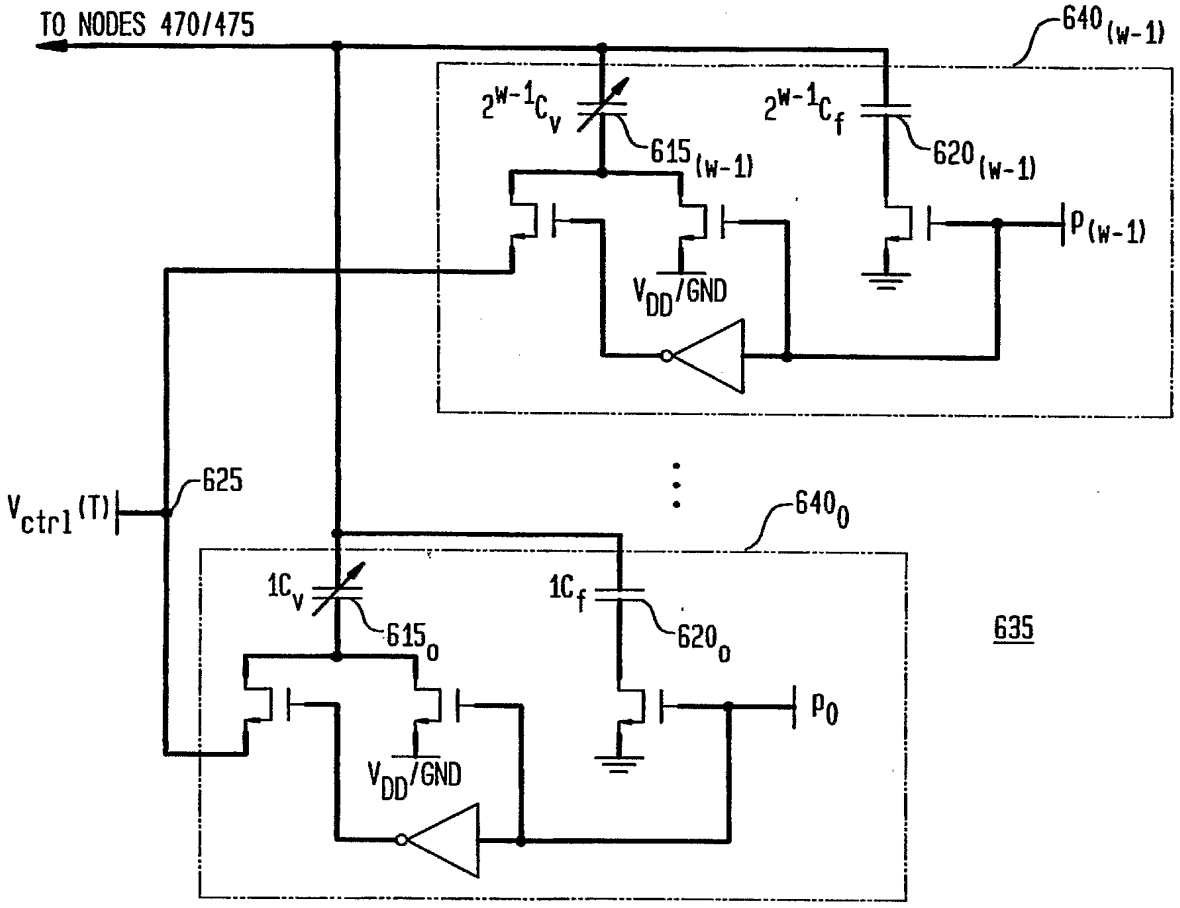

TO NODES 470/475
640(w-1)
2w-1Cv
615(w-1)
2w-1Cf
620(w-1)
P(w-1)
VDD/GND
Vctrl(T)
625
6400
1Cv
6150
1Cf
6200
635
P0
VDD/GND

FIG. 10

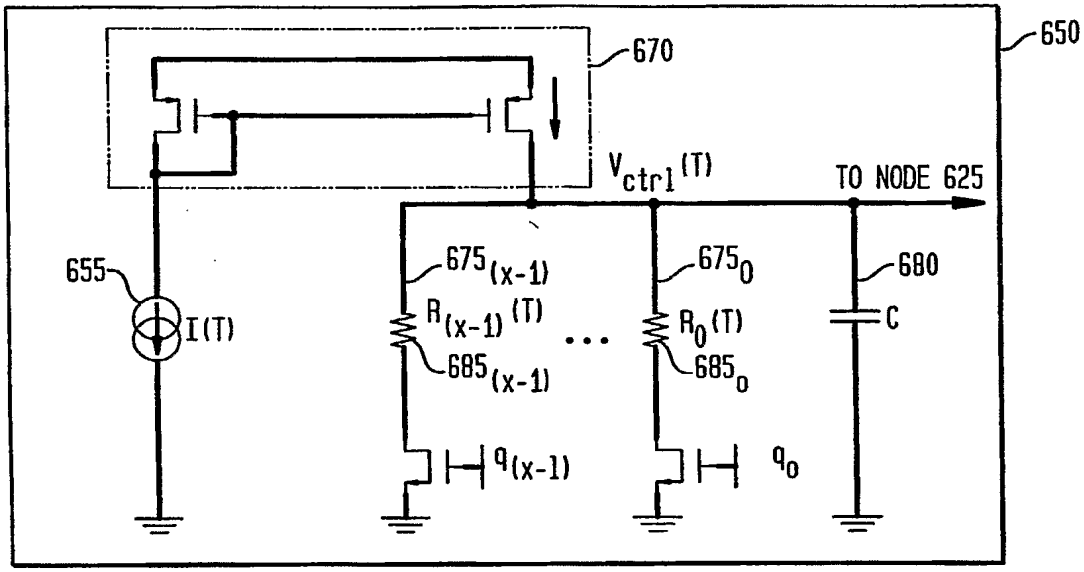

650
670
$V_{ctrl}(T)$
TO NODE 625
655
I(T)
$675_{(x-1)}$
$R_{(x-1)}(T)$
$685_{(x-1)}$
675_0
$R_0(T)$
685_0
680
C
$q_{(x-1)}$
q_0

FIG. 11

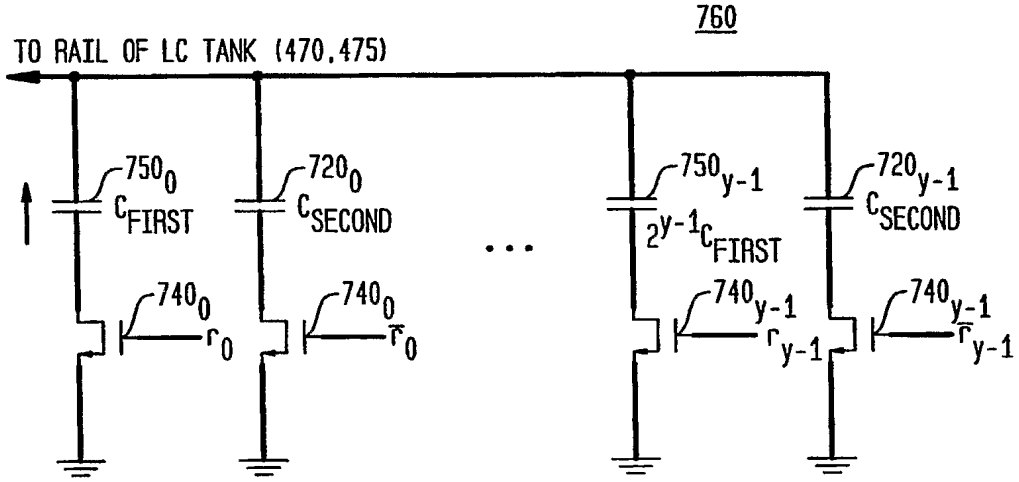

760
TO RAIL OF LC TANK (470,475)
750_0
C_{FIRST}
720_0
C_{SECOND}
740_0
r_0
740_0
r_0
750_{y-1}
$2^{y-1}C_{FIRST}$
720_{y-1}
C_{SECOND}
740_{y-1}
r_{y-1}
740_{y-1}
r_{y-1}

FIG. 12

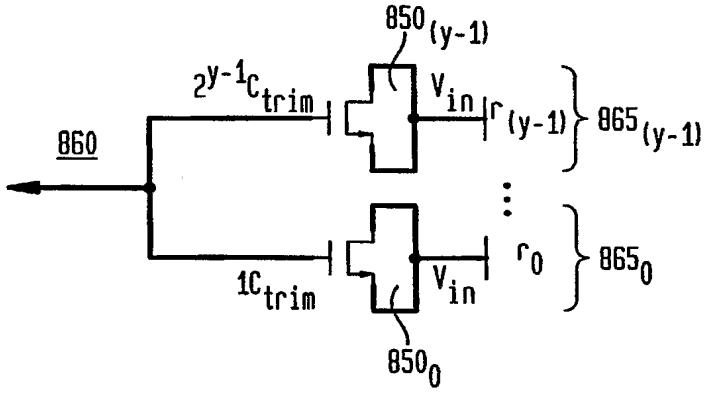

850(y-1)
2y-1Ctrim
Vin
r(y-1)
865(y-1)
860
1Ctrim
Vin
r0
865₀
850₀

FIG. 13

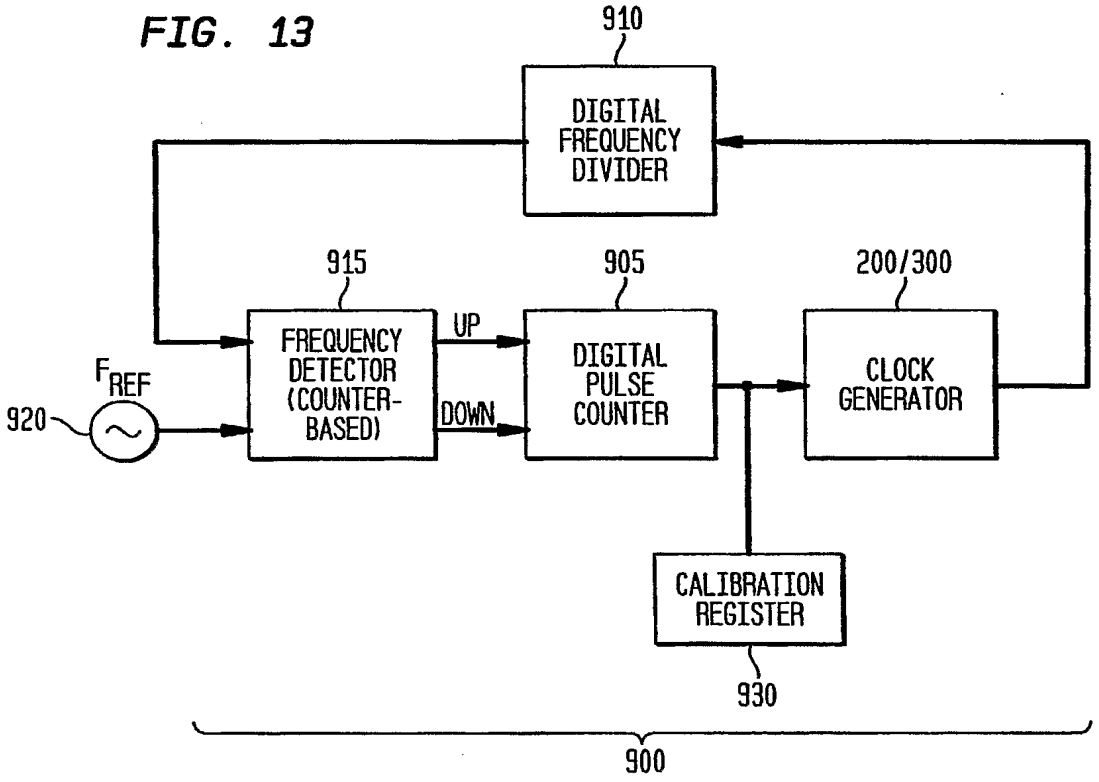

910
DIGITAL FREQUENCY DIVIDER
915
905
200/300
FREQUENCY DETECTOR (COUNTER-BASED)
UP
DOWN
DIGITAL PULSE COUNTER
CLOCK GENERATOR
FREF
920
CALIBRATION REGISTER
930
900

FIG. 14

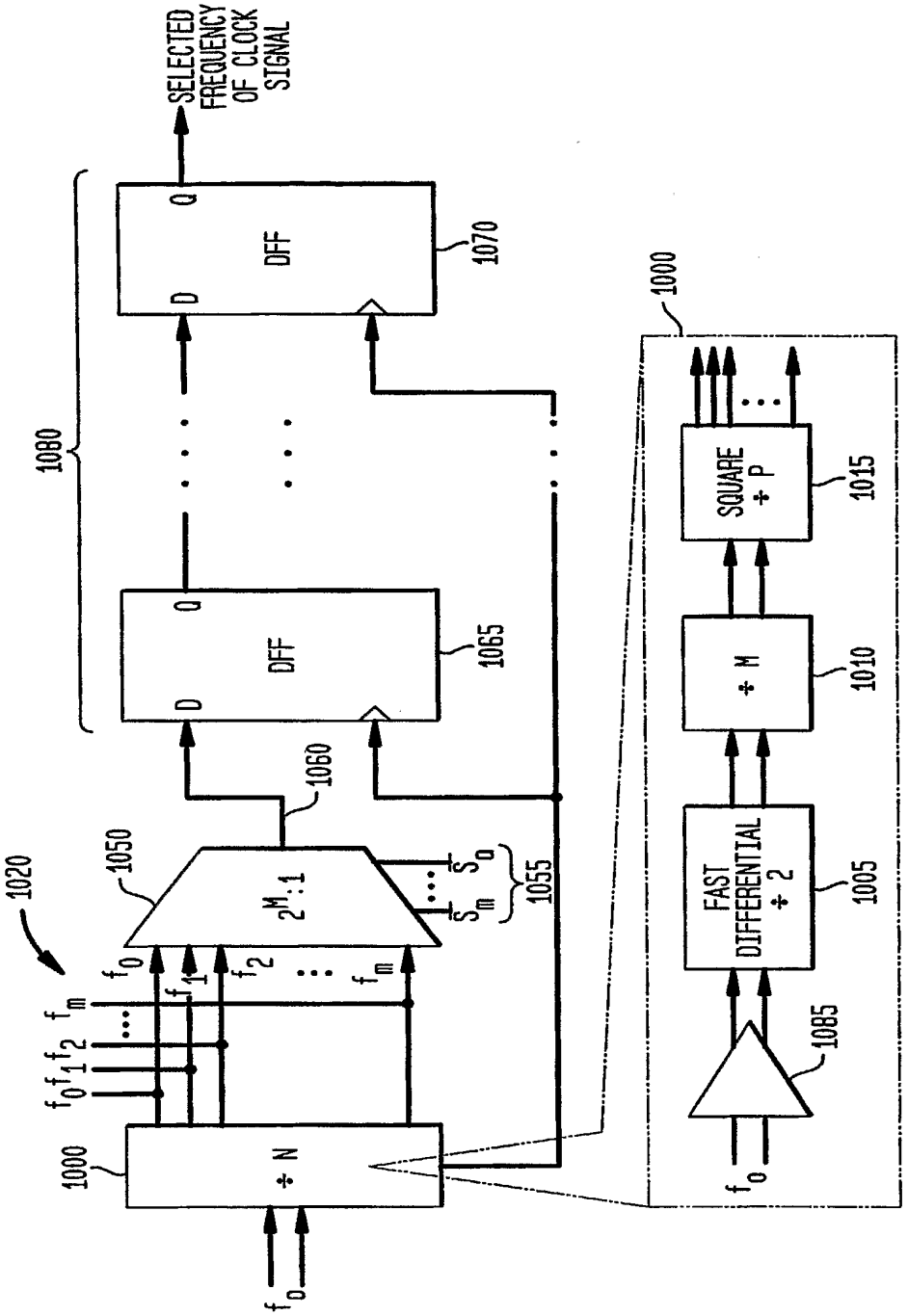

SELECTED FREQUENCY OF CLOCK SIGNAL
Q
D
DFF
1070
1080
1065
1060
1050
2^M:1
1020
1055
1000
÷ N
÷ M
1010
SQUARE ÷ P
1015
FAST DIFFERENTIAL ÷ 2
1005
1085

FIG. 15B

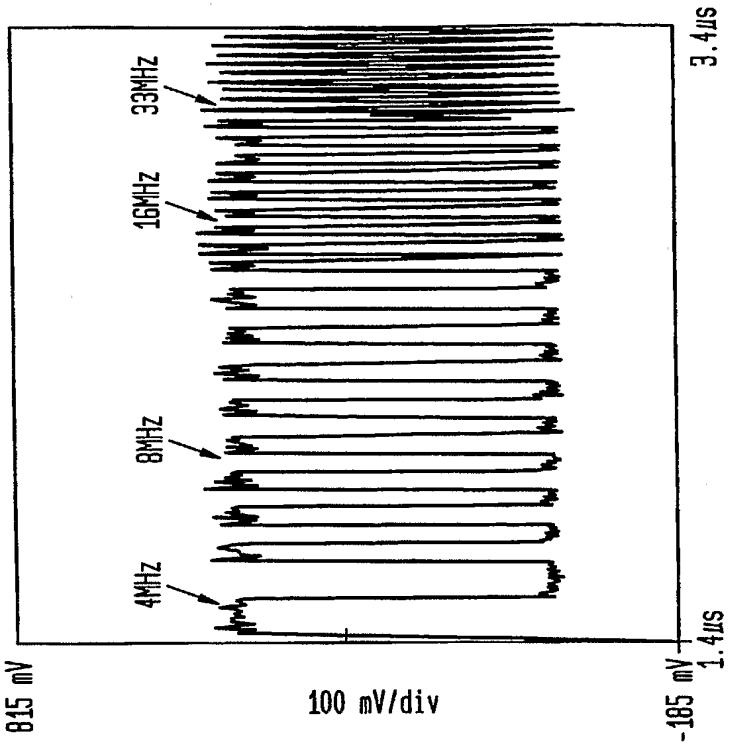


FIG. 15A

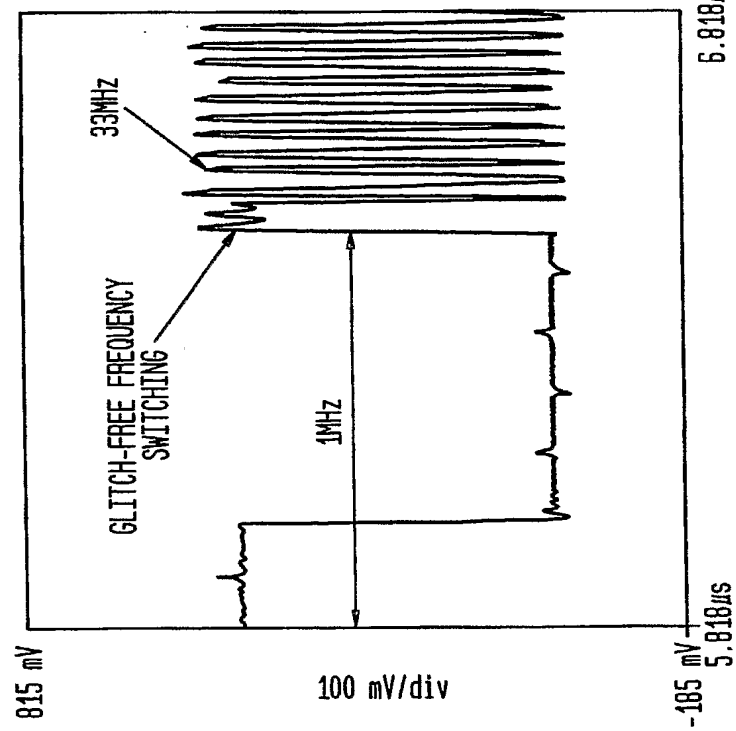


FIG. 16

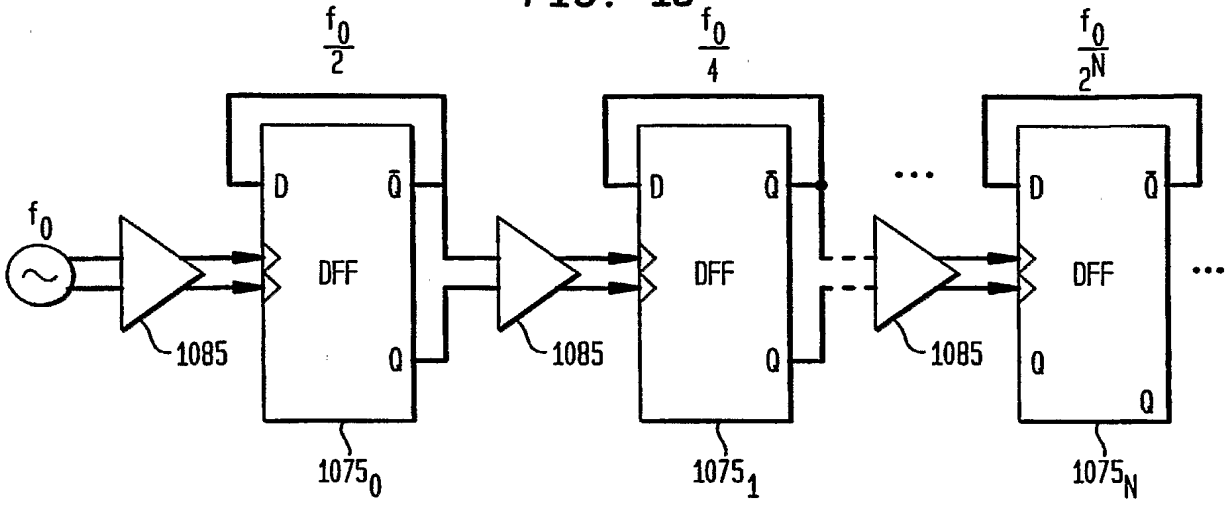


FIG. 17

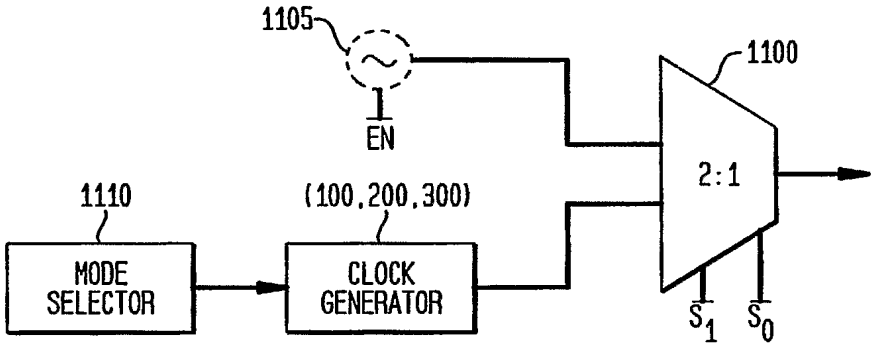


FIG. 18

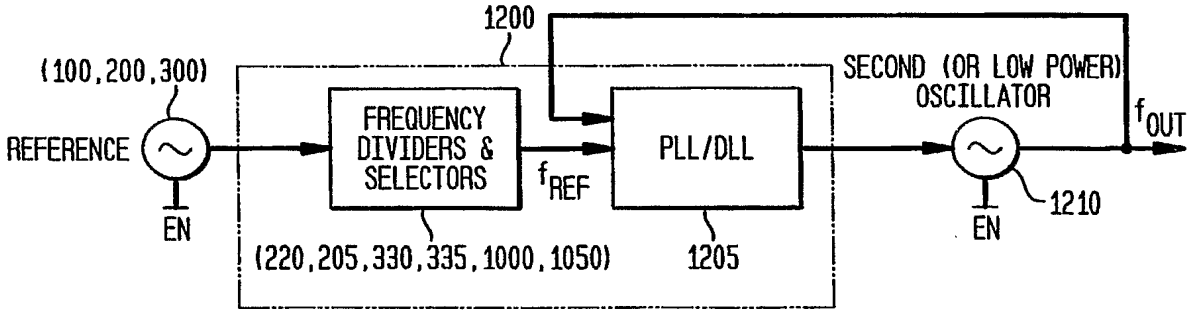
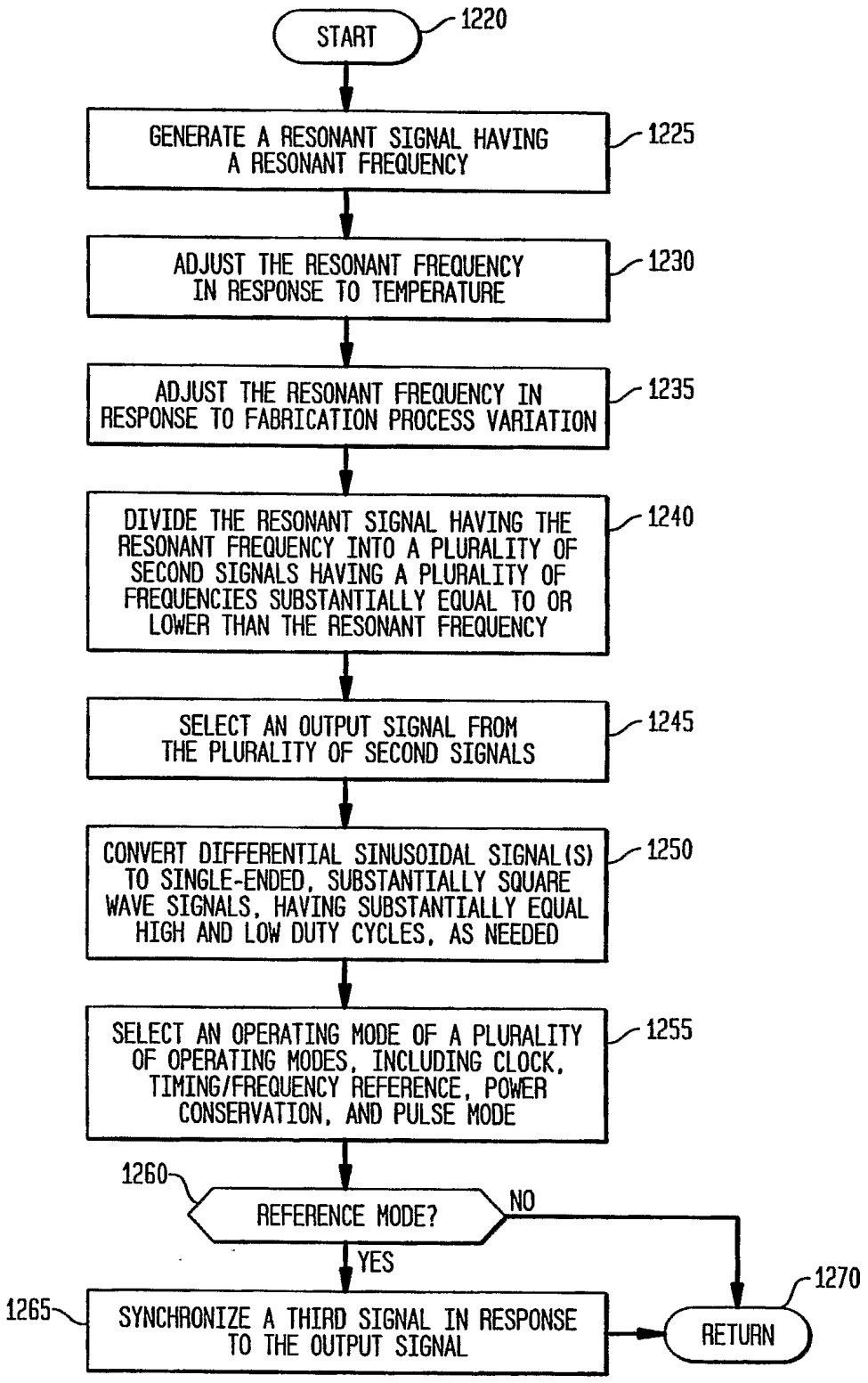


FIG. 19


START
1220
GENERATE A RESONANT SIGNAL HAVING A RESONANT FREQUENCY
1225
ADJUST THE RESONANT FREQUENCY IN RESPONSE TO TEMPERATURE
1230
ADJUST THE RESONANT FREQUENCY IN RESPONSE TO FABRICATION PROCESS VARIATION
1235
DIVIDE THE RESONANT SIGNAL HAVING THE RESONANT FREQUENCY INTO A PLURALITY OF SECOND SIGNALS HAVING A PLURALITY OF FREQUENCIES SUBSTANTIALLY EQUAL TO OR LOWER THAN THE RESONANT FREQUENCY
1240
SELECT AN OUTPUT SIGNAL FROM THE PLURALITY OF SECOND SIGNALS
1245
CONVERT DIFFERENTIAL SINUSOIDAL SIGNAL(S) TO SINGLE-ENDED, SUBSTANTIALLY SQUARE WAVE SIGNALS, HAVING SUBSTANTIALLY EQUAL HIGH AND LOW DUTY CYCLES, AS NEEDED
1250
SELECT AN OPERATING MODE OF A PLURALITY OF OPERATING MODES, INCLUDING CLOCK, TIMING/FREQUENCY REFERENCE, POWER CONSERVATION, AND PULSE MODE
1255
1260
REFERENCE MODE?
NO
YES
1265
SYNCHRONIZE A THIRD SIGNAL IN RESPONSE TO THE OUTPUT SIGNAL
RETURN
1270